REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 12-17 and 23-36 are pending. Claims 12-17 and 23-36 stand rejected.

Claims 12, 23, and 30 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 12-17 and 23-36 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,765,258 of Wu et al. ("Wu").

Applicant respectfully submit that amended claim 12 is not anticipated by Wu under 35 U.S.C. § 102(e).

Applicant has amended claim 12 to read as follows:

> A flash memory cell comprising:
> a plurality of gate stacks formed on a substrate, and a plurality of active regions formed in the substrate, wherein each of the plurality of the gate stacks has a gate stack length and a gate stack width;
> an interlayer dielectric (ILD) deposited over the gate stacks and the active regions;
> a one-dimensional slot patterned over the gate stacks in the ILD, wherein the one dimensional slot is to provide access to the plurality of active regions; and
> a bit line formed in the slot, wherein the bit line is to contact the plurality of active regions through the slot, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

(Amended claim 12)(emphasis added)

Wu, in fact, discloses a plurality of common source conductive bit lines and a plurality of common-drain conductive islands being integrated with a plurality of bit lines (Abstract). More

specifically, Wu discloses that dielectric layers 317a are aligned to a plurality of active regions (col. 8, lines 17-18, **Figures 31(a)** and **31(b)**). In particular, Wu discloses

> FIG. 4 shows a top plan view of the contactless parallel common-source/drain conductive bit-line flash memory array, in which a cross-sectional view along a A-A' line is shown in FIG. 3I(a). From FIG. 4, it is clearly seen that the plurality of common-source conductive bit-lines (CSBL's) and the plurality of common-drain conductive bit-lines (CDBL's) are formed in parallel and transversely to the plurality of parallel STI regions; and the plurality of metal word-lines (WL's) integrated with the plurality of planarized control-gate conductive islands 314b are formed transversely to the plurality of common-source/drain conductive bit-lines (CSBL's/CDBL's).

(Col. 8, lines 44-60)(emphasis added)

Thus, Wu merely discloses conductive bit-lines that are formed in parallel and transversely to the plurality of parallel STI regions, in contrast to a one-dimensional slot patterned over the gate stacks in the ILD, wherein the one dimensional slot is to provide access to the plurality of active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width, as recited in amended claim 12.

Additionally, Wu fails to disclose a bit line formed in the ILD slot, wherein the bit line is to contact the plurality of active regions through the slot, as recited in amended claim 12.

Because Wu fails to disclose all limitations of amended claim 12, applicant respectfully submits that amended claim 12 is not anticipated by Wu under 35 U.S.C. § 102(e).

Given that amended independent claims 23 and 30 contain at least the limitations similar to those discussed with respect to amended claim 12, applicant respectfully submits that claims 23 and 30 are not anticipated by Wu under 35 U.S.C. § 102(e).

Given that claims 13-17, 24-29, and 31-36 depend from amended independent claims 12, 23, and 30 respectively, and add additional limitations, applicant respectfully submits that claims 13-17, 24-29, and 31-36 are not anticipated by Wu under 35 U.S.C. § 102(e).

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Tatiana Rossin at (408) 720-8300.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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